Preface

At some point in a digital communications receiver, the received analog signal must be sampled. This is true for any digital communications system, regardless of whether it is baseband or passband, and regardless of the modulation scheme being used. Sampling at the wrong times can have a devastating impact on performance. The process of synchronizing the sampler with the pulses of the received analog signal is known as timing recovery.

Conventional timing recovery techniques ignore the presence of the error-control code. Instead, they are based on a a phase-locked loop (PLL). They are adequate only when the operating signal-to-noise ratio (SNR) is high enough. However, recent advances in error-control codes have made it possible to communicate reliably at very low SNR. This means that conventional timing recovery must perform at an SNR lower than ever before. Because the conventional approach ignores the presence of the error-control code, they eventually become unviable when the SNR is low enough. This book describes and investigates new timing recovery architectures that are able to exploit the presence and power of error-control codes, thus enabling reliable performance even at low SNR.

The ideas in this book stem from a research project conducted at the Georgia Institute of Technology, culminating in the Ph.D. dissertation "Timing recovery based on per-survivor processing" released in October 2004. The original focus was on magnetic recording channel, but the ideas are more broadly applicable to all baseband and passband communications systems. Therefore, this book presents the concept of iterative timing recovery in its broadest terms, so as to highlight its versatility. Although our scope is limited to timing recovery, the core concepts could be extended to encompass other synchronization and estimation tasks as well, such as carrier recovery. Therefore, we tried to present the concepts in basic terms so that the reader could apply them to whatever synchronization problem they are concerned with.

This book starts by defining the timing recovery problem. We explain the importance of timing recovery, and we argue that conventional timing recovery strategies are inadequate at low SNR, so that new timing recovery architectures are needed. Chapter 2 briefly describes how conventional timing recovery based on a PLL works. We describe how to design the parameters of a PLL using a linearized model. It is shown that for low to moderate SNR, conventional timing recovery does not perform well, especially when the timing error is large or when operating in a system that requires fast convergence. That is why new timing recovery architectures are required.

Chapter 3 describes a new timing recovery architecture based on per-survivor processing (PSP). Like conventional timing recovery, the approach in this chapter ignores the presence of error-control coding. But unlike conventional timing recovery, which operates separately from equalization, the proposed technique considers the timing recovery problem jointly with the equalization problem. Its architecture is fully explored and its performance is compared with conventional timing recovery.

Chapter 4 proposes a new timing recovery strategy that exploits the presence of error-control coding. Like the previous chapter, it too is based on per-survivor processing, but here the PSP is inserted into a turbo equalizer that jointly performs equalization and error-control decoding. Thus, we arrive at an iterative timing recovery scheme based on PSP that jointly performs timing recovery, equalization, and error-control decoding. It will be seen that this iterative timing recovery scheme outperforms the conventional receiver when operating at low SNR. This is because it can automatically correct a cycle slip. In addition, since performance analysis of iterative timing recovery schemes is difficult because of their complexity, this chapter also explains how to use the extrinsic information transfer (EXIT) chart analysis instead of bit-error rate to predict and compare their performances.

Although the iterative timing recovery scheme presented in Chapter 4 (referred to as the full-complexity scheme) outperforms the conventional receiver, its complexity is prohibitive in real-life applications. Therefore, a reduced-complexity iterative timing recovery scheme will be described in Chapter 5. For the same complexity, it will be illustrated that this reduced-complexity scheme performs better than the full-complexity scheme.

Chapter 6 is devoted to the application of magnetic recording systems. This application is important because magnetic recording is a primary method of storage for a variety of

applications, including desktop, mobile, and server systems. Timing recovery in magnetic recording systems is an increasingly critical problem because of the growing data rate to be supported. Improving the performance of timing recovery gives rise to improved reliability of an entire recording system, which in turn results in an increased storage capacity. Accordingly, this exercise will help us assess the applicability of the proposed timing recovery schemes in real-life applications, when compared to the conventional schemes used in today's magnetic recording read-channel chip architectures.

In Chapter 6, we begin with briefly reviewing the background of magnetic recording systems. A realistic magnetic recording channel model, which represents all the components that are employed in magnetic recording channels, is introduced. The method of designing the target and its corresponding equalizer is also given. Then, the timing recovery schemes presented in Chapter 3 – Chapter 5 are investigated and compared with the conventional schemes, based on the realistic magnetic recording channel model with and without error-control coding. Furthermore, the noise in magnetic recording channels is also data dependent. Media jitter noise can be given as an example of this type of noise, which depends on the data pattern written on the disk and can contribute a significant portion of the total noise. The pattern-dependent noise-predictive (PDNP) technique has been used to combat the pattern dependence of media noise. Consequently, a method to incooperate the PDNP technique inside the timing recovery architecture presented in Chapter 5 will be explained. We demonstrate that a large performance improvement can be obtained by using this technique, especially when operating in a channel at high normalized recording densities or at high media jitter noise levels.

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