After briefly describing conventional timing recovery in Section 27.2, we explain how to realize a fully digital timing recovery scheme and describe the design of the interpolation filters based on the minimum mean-squared error (MMSE) approach in Section 27.3. Implementation issues related to ITR are discussed in Section 27.4. Section 27.5 compares the performance of ITR with conventional timing recovery in magnetic recording channels under a variety of operating conditions. Finally, conclusions are given in Section 27.6.

27.2 Conventional Timing Recovery Architecture

Today's magnetic recording read-channel chip architecture uses conventional timing recovery to acquire synchronization. As shown in Figure 27.1, conventional timing recovery is based on a second-order PLL consisting of a timing error detector (TED), a loop filter and a VCO.

A decision-directed TED [1] is used to compute the estimated timing error, $\hat{\epsilon}_k$, which is the misalignment between the phase of the received signal and that of the sampling clock. Several TED algorithms have been proposed in the literature [1], depending on how they incorporate the information available at the TED input. In this chapter, we consider the well-known Mueller and Müller TED algorithm [2], which is expressed as

$$\hat{\epsilon}_k = y_k \hat{d}_{k-1} - y_{k-1} \hat{d}_k \tag{27.1}$$

where $y_k = y(kT + \hat{\tau}_k)$ is the kth sampler output, T is the bit period, $\hat{\tau}_k$ is the kth sampling phase offset adjusted by a PLL, and $\hat{d}_k$ is the kth desired sample.

Next, the estimated timing error is filtered by a loop filter to eliminate the noise in the timing error signal. Finally, the next sampling phase offset is updated by a second-order PLL according to

$$\hat{\theta}_k = \hat{\theta}_{k-1} + \beta \hat{\epsilon}_k \tag{27.2}$$

$$\hat{\tau}_{k+1} = \hat{\tau}_k + \alpha \hat{\epsilon}_k + \hat{\theta}_k \tag{27.3}$$

where $\hat{\theta}_k$ represents the frequency error, and α and β are the PLL gain parameters. Note that the PLL gain parameters determine the loop bandwidth and the rate of convergence. The larger the value of PLL gain parameters, the larger the loop bandwidth, the faster the convergence rate, and thus the more the noise allowed to perturb the system. Practically, a known data pattern called a *preamble* (or a training sequence) is usually sent during acquisition mode to help PLL achieve fast synchronization. Since this preamble is known at the receiver, large values of α and β can be used to expedite the convergence rate. However, the values of α and β should be lowered during tracking mode so as to reduce the effect of the noise [3]. Therefore, designers must tradeoff between the loop bandwidth and the convergence rate when designing α and β.

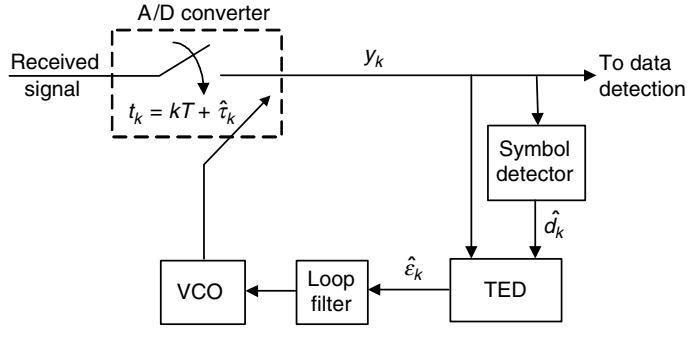

FIGURE 27.1 A conventional VCO-based timing recovery.